APPENDIX A

"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

SPECIFICATION:

Replacement for the paragraph beginning at page 10, line 12 to page 10, line 15:

It has been found that the stripe geometry will produce a larger channel width per unit area for polyline spacings in the region between about 1 to 4 microns, particularly at about 1.5 microns, surprisingly with a relatively small increase in Q_g.

CLAIMS (with indication of amended or new):

9. (Twice Amended) The process of manufacture of a MOSgated device comprising:

forming a gate oxide layer atop a silicon surface of one conductivity type;

forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said oxide; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of polysilicon as a mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; diffusing second base diffusion stripes, into said silicon surface, using said stripes of polysilicon as a mask, to a depth below that of said source diffusions and a width substantially equal to the space between the opposite edges of adjacent pairs of said polysilicon stripes.

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~~16.~~ (NEW) The process of claim 9 wherein said polysilicon stripes are spaced 1.5 microns apart.

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~~17.~~ (NEW) The process of claim 9 wherein said polysilicon stripes are spaced 3.2 to 3.4 microns wide.